

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office at facsimile no. (703) 308-6296.

**PATENT**  
Attorney Docket No.: 19705-000100US

On August 10, 2001

By: Gary T. Aka

Gary T. Aka

#14/C  
KWS  
8-17-01

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

**Bulent Dervisoglu et al.**

Application No.: 09/275,726 ✓

Filed: March 24, 1999

For: ON-CHIP SERVICE PROCESSOR  
FOR TEST AND DEBUG OF  
INTEGRATED CIRCUITS

Examiner: D. Ton

Art Unit: 2133



SUPPLEMENTAL  
AMENDMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

**OFFICIAL**

Sir:

In addition to the amendment of July 5, 2001 in response to the Office Action mailed April 4, 2001, please supplementarily amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claims 1, 10 and 15 as follows:

- 1 1. (Amended three times) An integrated circuit having logic blocks
- 2 comprising
- 3 a control unit for performing test and debug operations of said logic blocks of said
- 4 integrated circuit;
- 5 a memory associated with said control unit, said memory holding instructions for
- 6 said control unit; and
- 7 a plurality of probe lines responsive to said control unit for carrying system
- 8 operation signals from predetermined probe points of said logic blocks, wherein said probe lines
- 9 comprise strings of storage elements providing signal paths from said probe points to said
- 10 memory, said signal paths capable of moving sets of said system operation signals at system